Low-power All-analog Circuit for Rectangular-type Analog Joint Source Channel Coding

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***Abstract*—A low-complexity and low-power all-analog circuit is proposed to perform efficiently Analog Joint Source Channel Coding (AJSCC). The proposed idea is to adopt Voltage Controlled Voltage Source (VCVS) to realize the rectangular-type mapping in AJSCC. The proposal is verified by Spice simulations as well as via breadboard and Printed Circuit Board (PCB) implementations. Field testing results indicate that the design is feasible for low-complexity and low-power systems such as wireless sensor networks for environmental monitoring.**

I. Introduction

Analog Joint Source Channel Coding (AJSCC) [1] can compress two or more sensor signals into one with controlled distortion while also being robust against wireless channel impairments. AJSCC adopts Shannon mapping as its encoding method [2]. Such mapping, in which the design of *rectangular (parallel) lines* can be used for 2:1 compression (Fig. 1), was first introduced by Shannon in his seminal 1949 paper [3]. Later work has extended this mapping to a *spiral type* as well as to N:1 mapping [4]. AJSCC achieves optimal performance in rate-distortion ratio, whereas to achieve such optimality using *separate* source and channel coding, complex encoding/decoding and long block-length codes would be required, causing delays and energy inefficiencies. Shannon mapping has the two-fold property of (1) compressing the sources (by means of N:1 mapping) and (2) being robust to wireless channel distortions as the noise only introduces errors along the parallel lines (or the spiral curve). AJSCC requires simple compression and coding at the transmitter, and low-complexity decoding at the receiver. In rectangular-type mapping, in order to compress the source signals ("sensing source point"), say Humidity and Temperature voltages (V_H, V_T), the point on the space-filling curve with minimum Euclidean distance from the source point is chosen ("AJSCC mapped point"), as illustrated in Fig. 1, via a simple projection on the curve. The transmitted signal is then the "accumulated length" of the lines from the origin to the mapped point, where the error introduced by the mapping is controlled by the spacing Δ_H between lines.

Existing AJSCC Circuits: Existing AJSCC solutions use *all-digital hardware*, and are power demanding and of high circuit complexity. For example, a Software-Defined Radio (SDR) system to realize AJSCC mapping has been reported in [5]. The mapping was also recently implemented in an optical digital communication system in [6]. Shannon-mapping encoding was adopted in [7] for a digital video transmission. No existing work has implemented AJSCC using an all-analog, low-complexity design.

Our Proposal: We are proposing a novel all-analog circuit to realize AJSCC and to achieve the objective of very low circuit complexity and power consumption. The proposal is based on the observation that the voltage of each level can be generated by Voltage Controlled Voltage Sources (VCVS), which output a voltage that is proportional to the input voltage; also, these sources can be switched on or off based on the input signal. Our contributions can be summarized as follows:

- Proposing the first *all-analog circuitry* for AJSCC for low-complexity and low-power applications;
- Verifying the circuitry and assessing its performance by Spice simulations as well as by prototype development via breadboard and Printed Circuit Board (PCB) hardware implementations.

Paper Outline: In Sect. II, we present our all-analog circuit realization of AJSCC; then, in Sect. III, we provide the circuit performance results from both Spice simulations and implementations; finally, in Sect. IV, we draw the conclusions.

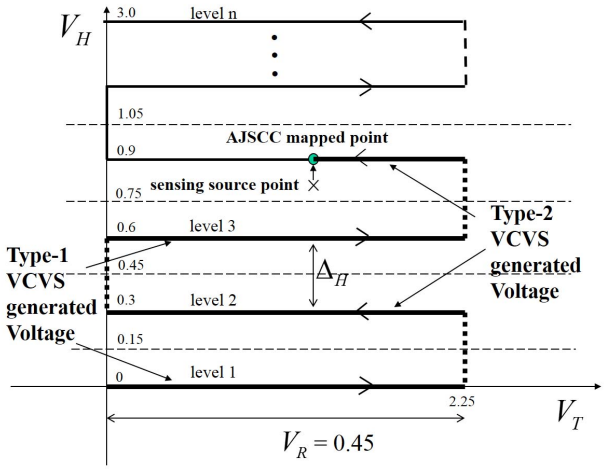


Fig. 1. **Shannon's Rectangular Mapping.** The sensed point is mapped to the point closest on the rectangular curve, and the accumulated length of the curve from the origin to the mapped point (in bold) is transmitted instead of the two values identifying the 2D sensed point. In our novel all-analog implementation, odd-level voltages are generated using Type-1 Voltage Controlled Voltage Sources (VCVS), whereas even-level voltages are generated using Type-2 VCVS. V_H and V_T are the humidity and temperature variable voltages, respectively, whereas V_R is a constant and Δ_H is the spacing between the levels. The numbers on the figure are the voltages used in Spice simulations.

II. All-analog Circuit Realization of AJSCC

Our proposed analog circuit is depicted in Fig. 2. The VCVS accepts voltage as input, and outputs a voltage that is a function of the input voltage. By observing the rectangular-mapping curve (see Fig. 1), there are two types of output increments. In the first (which we call Type 1), the output V_O

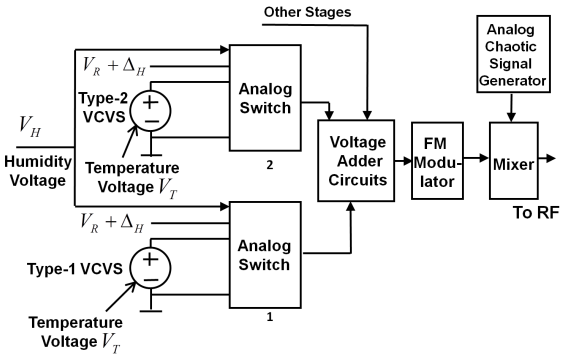


Fig. 2. **Proposed Analog Circuit for Shannon's Rectangular Mapping (only the first stage is shown)**. V_H is compared against threshold voltages to generate signals for the two analog multiplexers and decide which of the three inputs goes to the output. The outputs of both muxes are added to give this stage output. Similar outputs from higher stages are added to give the AJSCC encoded voltage, which is then frequency modulated (FM) and mixed with semi-orthogonal codes before the Radio Frequency (RF) transmission.

increases linearly with increasing V_T, i.e., $V_{O,Type1} \propto V_T$. This happens when we traverse the curve from left to right on odd-numbered lines to reach the mapped point. In the second (Type 2), the output decreases linearly with increasing V_T, i.e., $V_{O,Type2} = V_R - V_{O,Type1}$, which corresponds to traversing the curve from right to left on even-numbered lines to reach the mapped point. We realize these two types of outputs using two types of VCVS, where the overall mapping output is the voltage summation of the activated VCVS blocks, which represents the accumulated length of the curve from the origin to the mapped point. Note that V_H controls which VCVS levels/lines are activated, while V_T controls the VCVS output, as mentioned above. A stack of analog switches is used to implement the former and also to control the output of all levels. The number of switches is determined by the mapping resolution sought (Δ_H).

The first and second levels of the circuit are shown in Fig. 2, where the output of each level is controlled by the corresponding analog switch. Each switch has three inputs: $V_R + \Delta_H$, GND, and the output of either a Type-1 or Type-2 VCVS. V_R is a fixed voltage proportional to the x-axis range of the curve. Odd- or even-numbered switches are connected to Type-1 or Type-2 outputs, respectively. Note that the number of activated switches as well as the activation voltage of each switch are determined by considering both V_H and the chosen resolution Δ_H.

The switching logic is explained as follows: each switch is activated only if V_H is greater than a certain value based on the switch's level in the stack. If not activated, the output of the switch is connected to GND; if activated, the output is equal to the VCVS output within a certain range (Δ_H) of V_H above the activation voltage. Once V_H exceeds this range, the switch outputs its saturation voltage of $V_R + \Delta_H$. Finally, a voltage adder adds the outputs of all the (activated) switches and sends this analog signal to the FM analog circuit for Radio Frequency (RF) transmission. We refer the two levels, consisting of a Type-1 and Type-2 circuitry, as a *stage*. For sake of clarity, Fig. 2 represents only the first stage, which performs the mapping for the first two parallel lines (from the bottom).

In summary, if the mapped point lies on an odd-numbered line, i.e., if V_H is mapped to an odd-numbered level n, then the output of the voltage adder will be $V_O = (n-1)(V_R + \Delta_H) + V_T$; conversely, for an even level, the output will be $V_O = (n-1)(V_R + \Delta_H) + (V_R - V_T)$. As an example, for the highlighted point in Fig. 1, the output of the adder will be $3(V_R + \Delta_H) + (V_R - V_T)$. A Sallen-Key structure or a simple voltage divider can be used for Type-1 VCVS along with a subtractor for Type-2 VCVS, comparators to detect the V_H range, and a simple multiplexer for analog switching.

III. Circuit Performance Evaluation

In order to verify our design and to assess the performance of our AJSCC mapping circuit, we have carried out thorough Spice simulations as well as performed prototype development via breadboard and PCB hardware implementations.

Spice Simulations: The AJSCC mapping circuit has been simulated in Spice. As mentioned in Sect. II, our circuit consists of multiple identical stages stacked one on top of the other (i.e., hardware is duplicated). Each such stage consists of two levels—Type-1 and Type-2 VCVS-based circuitry. We considered a temperature sensor ($AD22100$) and humidity sensor ($HIH4000$) having range, respectively, $1.375-3.625$ V for $0-100°C$, and $0.8-3.8$ V for $0-100\%$. We first subtract the non-zero offset from V_T's range as it adds to the total mapped length without carrying information. We have also removed the offset from V_H as it simplifies the design; consequently, the offset-removed voltages, V_{T0} and V_{H0}, range in $[0, 2.25]$ and $[0, 3.0]$ V, respectively. Just for simulation and implementation purposes, we considered a 10% resolution in humidity giving us $\Delta_H = 0.3$ V. Since it is a second stage, Type 1 is in linear region (while Type 2 is OFF) when $0.45 \text{ V} < V_{H0} \leq 0.75$ V, and Type 2 is in linear region (while Type 1 is in saturation) when $0.75 \text{ V} < V_{H0} \leq 1.05$ V. These voltages are also shown in Fig. 1 for ease of understanding.

Figure 3 shows the detailed schematic of the second stage of our circuit simulated in LTSpice, a Spice simulation tool. While we have prototyped the entire system (Fig. 4), we have chosen to simulate only the second stage as the V_{H0} mapping range of both levels is more general compared to the first stage where the Type 1 has half of this value (i.e., 0 to 0.15 V). Offset removal is done using an OpAmp-based subtractor circuit. In fact, we have used well-known OpAmp-based subtractors and non-inverting adders for all subtractor and adder functionalities. Both V_T and V_H offset-removal blocks are indicated in the schematic. V_{H0} range comparison is achieved using Integrated Circuit (IC)comparators. Reference voltages (0.45, 0.75, and 1.05 V) for comparison are generated using a simple voltage-divider circuit, as shown in the figure. In each level (Type 1 or Type 2), the outputs of the comparators act as select lines for the analog multiplexer (switches), which receives three inputs, i.e., saturation voltage V_R, Type-1 VCVS output ($type1\_out$) for level 1 or Type-2 VCVS output ($type2\_out$) for level 2, and ground signal (g). Saturation voltage, V_R, is the output of Type-1 VCVS when the sensor senses the maximum temperature, i.e., when $V_{T0} = 2.25$ V. V_R and g signals are passed to the output of a Type-1 multiplexer when $V_{H0} \leq 0.45$ V and $V_{H0} > 0.75$ V, respectively. Similar statements hold for a Type-2 multiplexer.

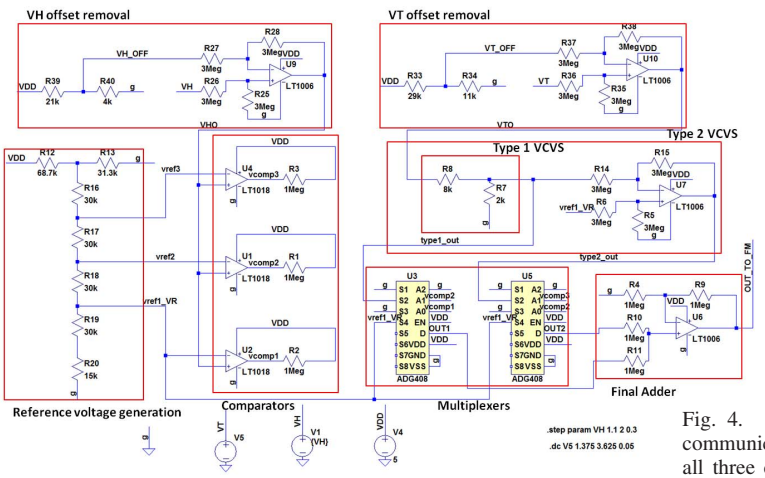


Fig. 3. **LTSpice schematic** of analog components of the second stage of the AJSCC-mapping analog circuit, where functional blocks are logically "boxed."

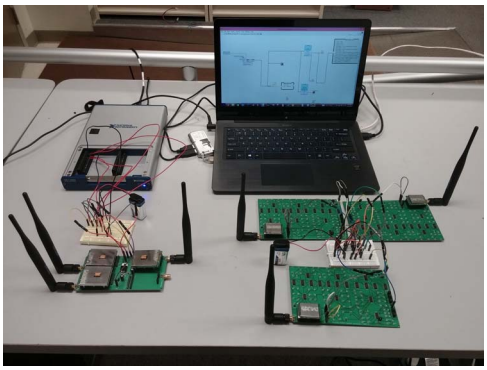


Fig. 4. **System prototype.** Three analog sensing boards (right bottom) communicating to an analog receiver (left bottom). The baseband signals of all three channels are captured using NI Digital Acquisition System (DAQ) (left top) and processed/decoded on a host laptop using LabView/MATLAB.

We have mentioned above the condition for V_{H0} when Type-1 (or Type-2) outputs are passed to the multiplexer. Type-1 VCVS is implemented as a simple voltage-divider circuit with 1:5 ratio, which means $V_R = 0.45$ V as $V_{T0,max} = 2.25$ V. The output of Type 1 is subtracted from V_R to get the Type-2 output.

Lastly, the outputs of both multiplexers are added to give the final output of this second stage. Similar outputs from the other stages are added to be given as input to the FM modulator. $V_R = V_1$ is determined by the maximum allowed voltage input to the FM modulator. We used manufacturer-provided Spice models to capture real performance; on the other hand, we were also limited by them as there are very few such models. Linear Technology's $LT1006$ and $LT1018$ as well as Analog Devices' $ADG408$ have been used, respectively, for OpAmp, comparator, and analog multiplexer functionalities.

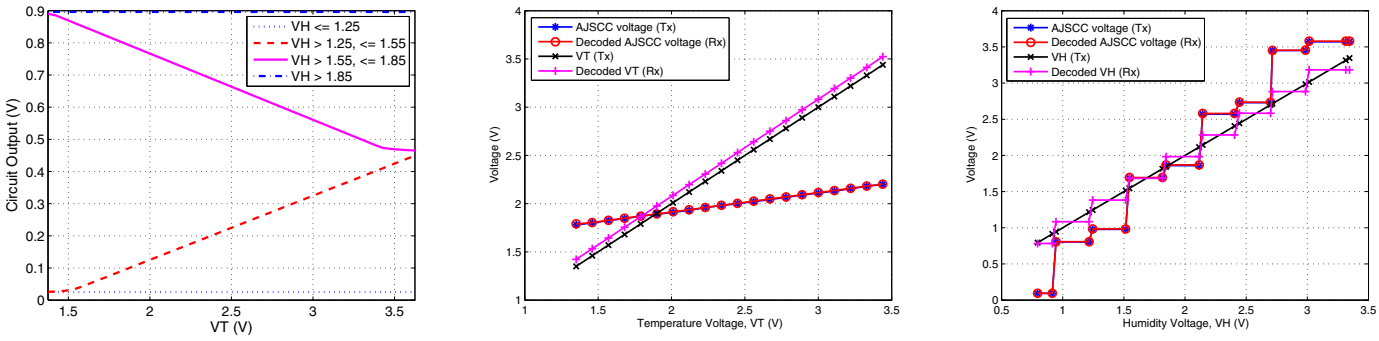
Figure 5(a) shows the output of the second stage over its entire mappable range of V_T and V_H. It can be seen that the output is almost zero when V_H is below 1.25 V and that, when $1.25 < V_H \leq 1.55$, Type 1 mainly drives the output (with zero contribution from Type 2); conversely, when $1.55 < V_H \leq 1.85$, Type 2 mainly drives the output (with V_R contribution from Type 1); finally, when $V_H > 1.85$, the output is $2V_R$ (i.e., V_R from each VCVS). Note that these are the actual sensor output voltages and not offset-removed values. Consequently, this circuit captures and maps the sensor outputs in the range $1.25 \leq V_H < 1.85$ and $1.375 \leq V_T \leq 3.625$. We can observe some saturation behaviors (output not being exactly zero) when both levels are inactive and at the beginning of Type-1 and Type-2 active modes, which we attribute to the saturation of the OpAmps.

Breadboard and PCB Hardware Implementations: We have also implemented this single stage on a breadboard to verify the reproducibility of the simulation results using real hardware. We found that the results were very similar to our simulation counterparts, as depicted in Fig. 5(a), with less saturation effects in fact. Breadboard results motivated us to go even a step further and implement the full circuit (all stages) along with the RF part (as a COTS component) i.e., a full-fledged sensor on a PCB entirely designed by us (Fig. 4). This sensor consists of three major blocks—AJSCC encoding, DC-to-sine wave conversion circuit, and a RFIC module. The AJSCC encoding block takes temperature and humidity voltages as input, and outputs the AJSCC-encoded voltage. It implements 11 VCVS levels in total, as per the setup described above ($\Delta_H = 0.3$ V). The DC-to-sine wave block converts the AJSCC-encoded DC voltage to a sine wave, which will then be FM modulated and RF transmitted by the RFIC module. We have also designed a receiver consisting of a RFIC module and a NI Digital Acquisition (DAQ) system, and used LabView to process the decoded V_T and V_H values.

Figure 5(b) shows the sensor's AJSCC-mapped voltage for varying V_T (with V_H held constant at 1.83 V), while Fig. 5(c) shows it for varying V_H (with V_T held constant at 1.71 V). As expected, when V_H is fixed, we observe a linear increase in the AJSCC output as V_T is increased within its range. This is because of the linear VCVS functionality. However, a step output is expected when V_T is fixed while V_H is varied within its range. This is because all those V_H values between two threshold-level voltages are mapped to the same voltage. It can also been seen in both cases that the decoded AJSCC voltage is very close to the transmitted AJSCC voltage, i.e., $\hat{V}_T$ closely follows V_T, while, as expected, a step is observed in $\hat{V}_H$.

We measured our prototype's performance when three sensors (Tx) communicate simultaneously to a digital Cluster Head (Rx) using Frequency Division Multiple Access (FDMA). Figure 6 plots the SDR vs CSNR, where the former is the Signal-to-Distortion Ratio, i.e., the inverse in logarithmic scale of the Mean Square Error (MSE); and the latter is the Channel Signal-to-Noise Ratio, i.e., the SNR of the baseband signal at the output of the receiver RF module. SDR and CSNR are plotted by varying the Tx-Rx distance (with V_T and V_H fixed). As CSNR increases the SDR also increases, indicating the improved signal reconstruction performance.

Power and Cost Considerations: State-of-the-art sensor nodes consume ≈ 0.5 mA in active mode and a few μA in sleep mode with supply voltages in the range $1.8 - 3.0$ V, i.e., $0.9 - 1.5$ mW without taking into account the radio power: the active power consumption is mainly due to the microcontroller and Analog-to-Digital (A/D) conversions. In contrast, our all-analog sensor does not use power-hungry A/D's or microcontrollers. The current drawn by the AJSCC



(a) (b) (c)

Fig. 5. (a) Breadboard AJSCC output of the *second stage*; notice the four different regions – off, linear (Type-1 VCVS), linear (Type-2 VCVS), and saturation. (b) PCB AJSCC output for varying V_T with $V_H = 1.83$ V, note that the AJSCC output is linear with increasing V_T and that $\hat{V}_T$ closely follows V_T (average $\hat{V}_H$ is 1.98 V). (c) PCB AJSCC output for varying V_H with $V_T = 1.71$ V; note that the AJSCC output and $\hat{V}_H$ are discrete (average $\hat{V}_T$ is 1.72 V).

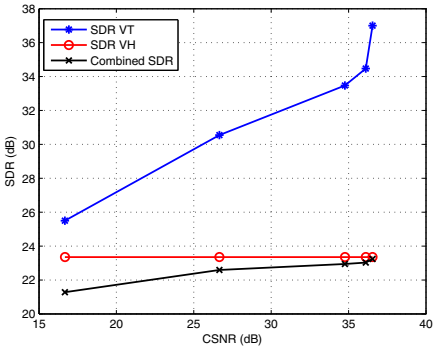


Fig. 6. SDR-vs-CSNR performance when three analog sensors (Tx) communicate simultaneously using AJSCC to a digital Cluster Head (CH), the receiver (Rx).

baseband circuitry (using COTS OpAmps, Multiplexers, etc.), i.e., the entire board excluding the RFIC module, is ≈ 3 mA with a supply voltage of 5 V (equivalent to ≈ 15 mW); the cost of the AJSCC PCB is about \$25. These numbers—which are high because of (1) the use of COTS components and (2) duplication of hardware for each stage—can be reduced *drastically* if state-of-the-art IC design is adopted. While our implementation serves as feasibility study, we are convinced that the power consumption can be reduced to ≈ 130 μW if our circuit is redesigned using the latest nm-technology components (for OpAmps, Comparators, and Multiplexers).

Let us provide a rough estimate: our circuit in total (5 and half stages/11 levels) consists of 16 OpAmps, 17 Comparators, and 11 Multiplexers, where OpAmps are clearly the major contributors to the overall power consumption. There are many low-power designs proposed for these components. For example, a low-power OpAmp [8] consuming about 8 μW, a comparator [9] consuming about 12.7 nW, and an analog multiplexer ($ADG704$) consuming about 10 nW can be used for our circuit resulting in a power consumption of ≈ 130 μW. We are also optimistic that the sensor cost would reduce to less than \$5 leveraging economies of scale via mass production using the latest IC technology. Achieving both goals will enable critical futuristic applications such as persistent wireless sensing and Internet of Things (IoTs)-based solutions.

IV. Conclusion and Future Work

We proposed a novel all-analog circuit for rectangular-type Analog Joint Source Channel Coding (AJSCC) using Voltage Controlled Voltage Sources (VCVS). The objective of this design is to achieve low-power, low-complexity compression of sensor signals with controlled distortion while being robust to wireless channel impairments. The proposed idea was evaluated by Spice simulations as well as via breadboard and PCB implementations. Results indicate that the proposed circuit works as designed. We are now studying the performance of our system under multiple access, exploring high-dimensional mapping for increased compression, and trying to reuse the hardware of a single stage for all stages to avoid duplication.

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